What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate of a first conduction type;

a drain layer of the first conduction type, formed on a surface of said semiconductor substrate;

a channel region of a second conduction type opposite to the first conduction type which is formed on said drain region

a source region formed of the first conduction type, in said channel region;

a gate insulating film formed on said channel region;

a gate electrode formed on said gate insulating film;

a recess formed in said source region so as to penetrate the source region and reach the channel region;

an insulating layer formed on a upper and side wall surfaces of the gate electrode; and

a wiring layer contacted with said source region and formed on the insulating layer.

2.The semiconductor device according to the claim 1,

further comprising a body contact region of the second conduction type, formed in a part of the channel region exposed in a bottom surface of the recess, wherein the wiring layer is contacted with said body contact region and said source region.

3.The semiconductor device according to the claim 1, wherein the insulating layer is constituted by an upper insulating layer and a side wall insulator, the recess is formed in align with the edge of the side wall insulator.

4.The semiconductor device according to the claim 3, wherein the body contact region is separated from the source region.

5.The semiconductor device according to the claim 1, further comprising a trench formed in said channel region, wherein said gate insulating film is formed on an inner wall of the trench and on the substrate main surface, and said gate electrode is embedded in the trench and reach to the substrate main surface.

6.The semiconductor device according to the claim 5, wherein the insulating layer is constituted by an upper insulating layer and a side wall insulator, the recess is formed in align with the edge of the side wall insulator.

7.The semiconductor device according to the claim 6, wherein the body contact region is separated from the source region.

8.The semiconductor device according to the claim 5, wherein said channel region is formed on the entire surface of the drain layer.

9.The semiconductor device according to the claim 8, wherein the recess is selectively formed in a center portion of the source region and penetrate the source region.

10.The semiconductor device according to the claim 1, wherein said source region is constituted by plurality of regions respectively located in a matrix, and said gate electrode is formed in a lattice-like shape to surround the source regions.

11. The semiconductor device according to the claim 4, wherein the trench comprises a plurality of trenches formed in a matrix so as to be surrounded said source region.

12. A method of fabricating a semiconductor device, comprising the steps of:

forming a drain layer of a first conduction type on a surface of a semiconductor substrate of the first conduction type;

forming a first insulating film on said drain layer;

forming a first conductive layer on said first insulating film;

forming a second insulating film on said conductive

layer;

patterning said second insulating film, said conductive layer, and said first insulating film, to form a gate insulating film from said first insulating film, and a gate electrode from said first conductive layer;

implanting an impurity of a second conduction type opposite to the first conduction type into a surface of said drain layer with using said gate electrode as a mask, thereby forming a channel region of the second conduction type;

implanting an impurity of the first conduction type into said channel region with using said gate electrode as a mask, thereby forming a impurity region of the first conduction type ;

forming a third insulating film so as to cover a surface of the impurity region, side walls of said gate insulating film, said gate electrode, and said second insulating film, and an upper face of said second insulating film;

etching back said third insulating film to form a side wall insulator consisting of said third insulating film, by remaining said third insulating film selectively on side walls of said gate insulating film, said gate electrode, and said second insulating film;

etching the impurity region to form a recess so as to penetrate the impurity region, thereby forming a source region consisting of the impurity region; and

forming a second conductive layer on an entire surface, and patterning said second conductive layer, thereby forming a

wiring layer.

13. The method of fabricating a semiconductor device, according to the claim 12, wherein further comprising a step of introducing an impurity of the second conduction type into the bottom of the recess to form a body contact region of the second conduction after etching the impurity region prior to forming a second conductive layer.

14. The method of fabricating a semiconductor device, according to the claim 12, wherein the etching step comprises the steps of:

forming a mask pattern having an opening located in a center of the source region and cover an entire surface except for the opening before etching the impurity region;

etching the impurity region by using the mask pattern to form a recess shallower than the exposed surface of the impurity region so as to penetrate the impurity region, thereby forming a source region of the impurity region remained; and

introducing an impurity of the second conduction type into the bottom of the recess to form a body contact region of the second conduction.

15. The method of fabricating a semiconductor device, according to the claim 12, further comprising the steps of:

forming a fourth thick insulating layer on a surface of

the semiconductor substrate; and

patterning the fourth thick insulating layer so as to remain a peripheral region of the substrate, prior to forming the drain region.

16. A method of fabricating a semiconductor device, comprising the steps of:

forming a drain layer of a first conduction type on a surface of a semiconductor substrate of the first conduction type;

introducing an impurity of a second conduction type opposite to the first conduction type into an entire surface of said drain layer, thereby forming a channel layer;

forming a trench so as to penetrate said channel layer and reach said drain layer using a first mask;

forming a first insulating film on an inner wall of said trench and a surface of said channel layer;

forming a conductive layer on said first insulating film;

forming a second insulating film on said conductive layer;

patterning said second insulating film, said conductive layer, and said first insulating film with using a same second mask, to form a gate insulating film of said first insulating film, and a gate electrode of said conductive layer;

implanting an impurity of the first conduction type into a surface of said channel layer with using said gate electrode as a mask, thereby forming a impurity region of the first

conduction type;

forming a third insulating film on an entire surface;

etching back said third insulating film to form a side wall insulator which covers side walls of said gate insulating film, said gate electrode, and said first insulating film;

forming a third mask having an opening located in a center of the source region and cover an entire surface except for the opening, before etching the impurity region;

etching the impurity region by using the third mask to form a recess shallower than the exposed surface of the impurity region so as to penetrate the impurity region and reach to the channel region, thereby forming a source region consisting of the impurity region; and

implanting an impurity of the second conduction type into a bottom of said recess, with remaining said third mask , thereby forming a body contact region; and

removing said third mask; and

forming a second conductive layer which covers said source region, said body contact region, said side wall insulator, and said second insulating film, and patterning said second conductive layer by using a fourth mask, thereby forming a wiring layer.

17. The method of fabricating a semiconductor device according to claim 16, wherein said step of forming a source region is formed before the step of forming a trench.